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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/639,058	08/11/2003	Andrew E. Horch	2000.004.00/US	6760

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WALTER D. FIELDS
FIELDS IP, PS
601 MAIN STREET
SUITE 405
VANCOUVER, WA 98660

EXAMINER	
TRINH, HOA B	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/639,058	HORCH, ANDREW E.	
	Examiner	Art Unit	
	Vikki H. Trinh	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-101* is/are pending in the application.

4a) Of the above claim(s) *20-101* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5-19* is/are objected to.

8)☒ Claim(s) *1-101* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0305*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 20-101 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected groups, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 01/07/05.

2. It is suggested that in response to this Office Action, applicant should cancel claims 20-101.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (hereinafter "Chen") "Fabrication of Self-Aligned 90-nm Fully Depleted SOI CMOS SLOTFETS".

Chen discloses, as to claim 1, method of fabricating a thyristor memory, comprising: forming sidewalls (fig. 1, steps (a) and (b)) in a layer of dielectric (fig. 1, step (a)) over a layer of semiconductor material (fig. 1, step (a)) to define a trench (fig. 1, step (a)) and expose a region (fig. 1, step (b)) of the semiconductor material through the opening of the trench; forming conductive material (fig. 1, step (c)) on at least portions of the dielectric and in the trench; patterning the conductive material to define first and second shoulders (fig. 1, step (d)) extending

outwardly from the trench over regions of the dielectric outside the trench; the patterning to comprise forming the first shoulder (fig. 1, step (d)) as an overhang extending laterally outward from the trench over regions of the layer of semiconductor material for the thyristor; etching exposed regions (fig. 1, step (e)) of the layer of dielectric to form an implant mask (fig. 1, step (d)) while using the conductive material with the first and second shoulders as an etch mask (fig. 1, step (d)), implanting regions (fig. 1, step (d)) of the layer of semiconductor material; and using the implant mask (fig. 1, step (e)) to align placement of dopant during at least a portion of the implanting.

As to claim 2, the implanting comprises performing a first implant (col. 2, line 2) of first conductivity type dopant.

As to claim 3, the first implanting (fig. 1, step (d)) comprises penetrating with the dopant of the first conductivity type regions (col. 2, line 2) of the layer of semiconductor material beneath an edge of the implant mask.

As to claim 4, the first implanting (fig. 1, step (d)) comprises forming a base region to the thyristor; and forming at least a portion of the base region beneath the first shoulder (fig. 1).

Allowable Subject Matter

3. Claims 5-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is an examiner's statement of reasons for allowance: The prior art of record does not disclose or fairly suggest either in singly or in combination a method of making a thyristor memory comprising the steps of etching exposed regions of the dielectric layer to form

an implant mask while using the conductive material with the first and second shoulders as an etch mask; using the implant mask to align placement of dopant during at least a portion of the implanting; performing a second implant of the second conductivity type dopant aligned with the implant mask and forming an anode/cathode-emitter; and other steps in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign

patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Vikki Trinh,
Patent Examiner
AU 2814

HOWARD WEISS
PRIMARY EXAMINER